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Skills overview

Hardware

Able to design scholastically tested VHDL/Verilog models for ASICs and FPGAs trading off area, speed and power consumption. System on Chip architecture and communication design using e.g. CoreConnect or AMBA. Able to design moderate analog and mixed-signal systems for instrumentation and control including schematic capture, simulation and PCB (OrCAD). Creating compact VLSI layouts that meet timing and power constrains. Software packages:

ASIC/FPGA flows: Xilinx's XPS and ISE, Leonardo Spectrum, Cadence's BuildGates/PKS.
Physical-Layout: Silicon Ensemble, L-Edit, Magic, Cadence's Virtuoso (basic knowledge).
Simulation-modeling: Digital: Modelsim, SimVision. Analog: Spice. System-level: Matlab, Labview.

Software

Developing firmware for embedded and mobile applications. Capable with DSP algorithms for audio and video processing. Interested in 3D graphics applications and algorithms. Experienced with higher level technologies including object oriented methodologies, databases, XML and distributed programming.

Processors: x86, ARM, PowerPC. Microcontrollers: AVR, PIC, TINI(8051). DSPs: BlackFin
Embedded OSs: Montavista Linux, Windows Mobile, FreeRTOS, Java VMs.
Languages: Embedded: C/C++, assembly, Java, C#. Scripting: bash, perl, Tcl/Tk

Soft skills

Have a unique ability to make things work through methodical planning and hard work. Proved experience in setting priorities to successfully meet strict deadlines. Able to lead small teams by communicating effectively, empathizing and understanding member's motives.

Education

2005 – 2006: University of Southampton, United Kingdom

MSc in Microelectronic System Design. System on Chip stream, GPA: 83%, Distinction, Zepler prize for outstanding academic achievements.

Thesis: "Core Services: A new design methodology for Multiprocessor System-on-Chips"

1999 – 2004: National Technical University of Athens, Greece

5 year diploma in Applied Mathematics and Physics. Optoelectronics and laser stream, GPA: 74%.

Thesis: "Applications of Radon transform in Image Recognition and implementation on DSP"

Work experience

January - August 2005, NAMA Geoinformatics S. A., Greece

Mobile Application Engineer

Developed a GPS tracking application for ARM powered PocketPCs. Requirements analysis, design specification, spatial compression and filtering algorithm design, development in C# and .NET CF.

December 2003 – September 2004, NAMA Geoinformatics S. A., Greece

Application Engineer

Developed the client tier for the Geographic and Descriptive Database of the Olive and Vineyard Registry of Greece. This GIS Java front end is now being used by the Ministry of Agriculture of Greece.

June – August 2003: CERN, Geneva

Summer Student

Developed data logger for data acquisition system of the Atlas muon detector on the LHC accelerator at CERN. Design specification, development in Java.

January 2003 – March 2004, Thalix S.P., Greece

Embedded Application Engineer

Designed the digital part and the firmware for a power factor correction module. Requirements analysis, digital system design, firmware in C.

2001-2004, May - September 2005, Main Studio S.P., Greece

Partnership

Developed an embedded MP3 player that evolved to a DJ solution with on-line voting via web and kiosks. Requirement analysis, components evaluation and integration, real-time audio processing algorithms, development in C++ under Linux.

Academic projects and publications

Core services: A new design methodology for MPSoCs (Dissertation)

Extended Xilinx's high-end FPGA platform with a Web Services inspired mechanism for interoperable on-chip communication which supports dynamic reconfiguration, fault tolerance and run-time mapping. CoreConnect platform wrappers, device drivers for MontaVista embedded Linux, development and platform integration of high-performance accelerating cores for MP3 decoding and AES encryption.

Software Power Estimation (Score 93%)

Developed a power estimation component for profiling and simulation tools like gprof and bochs able to give estimates with application up to OS-level granularity. Used C++, perl, IA-32 assembly for Linux.

VLSI design project (Score 86%)

Led my team to the design of the second best full custom processor of the course. It is thoroughly tested and accompanied with SimVision Tcl-Tk visualization plug-in and AT&T compatible assembler.

Timing Attacks on Cryptosystems: RSA (Score 97%)

An enhanced version of Kocher's timing attack on RSA cryptography scheme evaluated with three different timing models for modular exponentiation.

Application of Radon transform in Image Recognition and implementation on DSP (Dissertation)

Implemented the firmware for a standalone image recognition device using Analog Devices' Blackfin DSP. It captures and processes real-time video and presents the results on any PAL screen.

S. Maltezos, E. Fokitis, D. Kouzis-Loukas, R. Liarokapi, High performance multilayer notch optical filters for high energy detector application and their coating process control, in the proceeding of the 8th International Conference on Advanced Technology and Particle Physics (ICATPP), 2003

Designed the data acquisition module for a high-speed multi-channel spectrograph and the simulation software for the coating process. Analog and digital design, firmware, OrCAD, Matlab, Labview.

Further information

Details about projects

Details about projects can be found on my web site: <http://www.lookfwd.doitforme.gr/projects>

Referees

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